UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GLEN D. WILK, ROBERT M. WALLACE and BERINDER P.S. BRAR

Appeal No. 2005-1552
Application No. 09/176,422

ON BRIEF

Before HAIRSTON, KRASS, and JERRY SMITH, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 25.

The disclosed invention relates to a low temperature method for forming a thin gate oxide on a clean silicon surface.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A low temperature method for forming a thin gate oxide on a silicon surface, the method comprising:

providing a partially completed integrated circuit on a semiconductor substrate with a clean, atomically flat, silicon surface;

stabilizing the substrate at a first temperature no greater than about 200 degrees C;

exposing the silicon surface to an atmosphere including ozone, while maintaining the substrate at the first temperature, wherein the exposing step creates a first, uniformly thick, gate oxide film.

The references[1] relied on by the examiner are:

Faraone et al (Faraone)	4,604,304	Aug. 5, 1986
Doklan et al. (Doklan)	4,851,370	Jul. 25, 1989
Cook et al. (Cook)	5,194,397	Mar. 16, 1993
Choquette et al. (Choquette)	5,275,687	Jan. 4, 1994
Fujishiro et al. (Fujishiro)	5,294,571	Mar. 15, 1994
Wilk et al. (Wilk)	6,020,247[2]	Feb. 1, 2000

Nayar, "Atmospheric Pressure, Low Temperature (<500°C) UV/Ozone Oxidation Of Silicon," Electronics Letters, 26(3), pp. 205-06 (Feb. 1, 1990).

Wolf, "Thin Gate Oxides: Growth and Reliability," Silicon Processing for the VLSI Era - Volume 3: The Submicron Mosfet, pp. 422-23 (Lattice Press, 1995).

Claims 1 through 25 stand rejected under the first paragraph of 35 U.S.C. § 112 for lack of enablement.

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[1] The references to Cook, Faraone and Doklan are listed by the examiner (answer, page 3), but are not applied in the rejections of record.

[2] U.S. Patent Number 6,020,247 to Wilk is incorporated by reference on page 1 of the subject application.

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujishiro in view of Nayar.

Claims 24 and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujishiro in view of Nayar and Wolf.

Claims 1 through 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujishiro in view of Nayar and Choquette.

Claim 23 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujishiro in view of Nayar, Choquette and Wolf.

Reference is made to the second supplemental brief and the answer for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse all of the rejections of record.

Turning first to the lack of enablement rejection, it appears that the examiner is trying to establish a case of lack of enablement based upon the allegedly identical teachings of Nayar. We are not aware of any solid grounds upon which the examiner can make such a rejection. Since the record before us completely lacks a finding that the teachings of Nayar and the disclosed and claimed invention are identical, any perceived

attack upon the teachings of Nayar can not be translated by the examiner into an admission by appellants that their own disclosure lacks enablement. With respect to the examiner's concerns (answer, pages 8 and 9) about "an atomically flat Si substrate," we agree with the appellants' statement (second supplemental brief, page 7) that the incorporated by reference patent to Wilk discusses how to make such a silicon surface. In summary, the rejection of claims 1 through 25 under the first paragraph of 35 U.S.C. § 112 is reversed because none of the reasons expressed by the examiner supports a lack of enablement rejection.

Turning next to the obviousness rejection of claim 18, we disagree with the examiner's finding (answer, page 4) that "Nayar anticipates growing an ultra-thin gate oxide, by UV formed ozone ambient, for microelectronic use, p. 206, bottom of first col., after a surface cleaning" (emphasis added). Nayar is completely silent as to a gate oxide, and he never mentions cleaning the silicon surface before forming the surface oxide by an ozone technique at a temperature below the temperature claimed by appellants. Since Fujishiro forms a gate oxide at temperatures above the claimed temperature, and is also silent as to a clean surface before forming the oxide, we agree with the appellants'

arguments (second supplemental brief, pages 8 through 10) that the applied references neither teach nor would have suggested to one of ordinary skill in the art the method steps of claim 18. Thus, the obviousness rejection of claim 18 is reversed.

The obviousness rejection of claims 24 and 25 is reversed because the breakdown voltage teachings of Wolf do not cure the noted shortcomings in the teachings of Fujishiro and Nayar.

Turning to the obviousness rejection of claims 1 through 13, the examiner turns to Choquette for a teaching of a process of forming "an atomically flat or smooth surface prior to the formation of a high quality epitaxial layer, see abstract" (answer, page 6). According to the abstract in Choquette, a contaminated III-V semiconductor surface (e.g., gallium arsenide), and not a silicon substrate, is subjected to sequential cleaning steps of exposure to hydrogen plasma, chemical etching in chloride and annealing in a vacuum to produce an atomically smooth surface. Appellants argue (second supplemental brief, page 11) that a method of cleaning a gallium arsenide surface has nothing to do with cleaning a silicon

surface. We agree with appellants' argument. Thus, the obviousness rejection of claims 1 through 13 is reversed because the applied references neither teach nor would have suggested an "atomically flat, silicon surface."

The obviousness rejection of claim 23 is reversed because the teachings of Wolf fail to cure the noted shortcoming in the teachings of Fujishiro, Nayar and Choquette.

DECISION

The decision of the examiner rejecting claims 1 through 25 under the first paragraph of 35 U.S.C. § 112 is reversed, and the decision of the examiner rejecting claims 1 through 13, 18 and 23 through 25 under 35 U.S.C. § 103(a) is reversed.

REVERSED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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) BOARD OF PATENT
ERROL A. KRASS)
Administrative Patent Judge) APPEALS AND
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